A NEW EFFECTIVE APPROACH FOR HIGH YIELD MICROWAVE MATCHING NETWORK AND AMPLIFIER DESIGN

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ABSTRACT: *In this paper, orthogonal array experiment of statistics is at the first time introduced to design high yield matching networks and select high yield topologies of matching networks for the load impedances located at the different regions on the Smith Chart. The circuit designed by this new approach always has a high yield. Also with this new approach, an FET amplifier is designed. Its performances are similar to those of the amplifier of [5],but its yield is much higher than that of the latter.*

1. INTRODUCTION

With the rapid development of MMIC, yield improvement becomes more and more important and computer-aided design of microwave circuits is turning the emphasis from the performance optimization to the yield optimization.Purviance *et al* [1],[2] studied the yield of the lumped 2-element and 3-element matching networks. They found that the yield relates not only to the nominal value and tolerance of the component,but also to the topology of the network. Generally, the topology affects the yield of the circuit more strongly than the nominal value and the tolerance.

When the operating frequency increases,the distributed and the mixed lumped-distributed matching networks are appreciated.So it is the intention of this paper to study the yield of these matching networks and the corresponding high yield topologies. Traditionally, Monte Carlo simulation is exploited for yield estimation. However, it can be rather expensive in computation. In any case, such simulations only enable the designer to estimate the yield of a given design. The general problem of statistical circuit design has not been fully solved.

Here, orthogonal array experiment (OAE) [3],[4], which has been widely used in quality control, is at the first time introduced as one of the feasible methods to design the high yield matching network and study the yield. In statistics, it has been proven to be an effective approach for experiment arrangement and result data analysis according to the orthogonal array.In this paper,circuit analysis is used instead of the experiment of OAE. The advantages of this new approach are that the tolerances of the components are considered and the average of an appropriate evaluation function is used as a yield measure for yield optimization to avoid time-consuming Monte Carlo simulation. In this way, the high yield topologies of matching networks are easily determined for the load impedances located at the different regions on the Smith Chart and the nominal value of the designed matching network is always the design center.

Finally, incorporating with OAE and the high yield topologies, a single-stage microwave FET amplifier is designed.Its performances are similar to those of the amplifier of [5], but its yield is much higher than that of the latter.

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2. HIGH YIELD MATCHING NETWORK STUDY

The distributed π matching network has four possible topologies as shown in Fig.1.Each of them can match any load impedance located on the Smith Chart. Before studying the yield of the matching network, the first problem has to be solved is how to design it. Usually, the design specification of the matching network is the input reflection coefficient, Γ_{in}. For the matching network of Fig.1 , Γ_{in} can be expressed as follow:

$$\Gamma_{in}=F(\tilde{Z}_i,\ l_i,\ \tilde{Z}_L,\ f) \qquad (1)$$

where $\tilde{Z}_i$, $i=1,2,3$ and $\tilde{Z}_L$ are the characteristic impedances and load impedance normalized by the source impedance Z_g respectively; l_i is the length of the ith transmission line and f is the operating frequency.

To study the relation between the yield and the topology of the matching network conveniently, the design method must be simple and valid. In this paper, OAE of statistics is applied for matching network design. It involves two iterative steps.

STEP 1. For a specific set of $\tilde{Z}_i$, $i=1,2,3$, determine the normalized length of ith transmission line, L_i, as follow:

Let the normalized load admittance be $\tilde{Y}_L=\tilde{G}_L+j\tilde{B}_L$ and the input admittance of the kth transmission

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line be $\tilde{Y}_{ink}$, K=1, 2, 3.

1) Let $\tilde{Y}_{in1} = -j\tilde{B}_L$. From this equation, determine L_1.

2) Let $\tilde{Y}_{in2} = \tilde{Y}_2 \dfrac{\tilde{G}_L + j\,\tilde{Y}_2\, tg(2\pi L_2)}{\tilde{Y}_2 + j\,\tilde{G}_L\, tg(2\pi L_2)} = 1+j\tilde{B}_2$,

where $\tilde{Y}_2 = 1/\tilde{Z}_2$. According to $Re(\tilde{Y}_{in2})=1$, determine L_2

3) Let $\tilde{Y}_{in3} = -j\tilde{B}_2$. From this equation, determine L_3.

STEP 2. Determine $\tilde{Z}_1$ using OAE as follow:

1) Select the orthogonal array $L_9(3^4)$ as optimizing array (also called internal array [4]), which is used to determine the best combination of $\tilde{Z}_i$. Select $\tilde{Z}_1$ as the factors (also called optimizing varibles) for optimizing array experiments. Let each factor has three levels. Genenally, there is a range for $\tilde{Z}_1$ selection. For example, the range for Z_i of the microstrip line is about 30 Ω to 100 Ω. Let Z_g= 50 Ω, then the levels of $\tilde{Z}_1$ and $\tilde{Z}_3$ can be selected as 0.6, 1.0 and 2.0. To satisfy $Re(\tilde{Y}_{in2})=1$, $\tilde{Z}_2$ must satisfy the constraint:

$$\tilde{Z}_2 \begin{cases} > 1/\sqrt{\tilde{G}_L} & \text{when } \tilde{G}_L > 1 \\ < 1/\sqrt{\tilde{G}_L} & \text{when } \tilde{G}_L < 1 \end{cases} \qquad (2)$$

Hence, when $\tilde{G}_L$>1. 0, the levels of $\tilde{Z}_2$ is seleced as $1/\sqrt{\tilde{G}_L}$ +0. 01, 1. 0, 2. 0 and when $\tilde{G}_L$<1, as 0. 6, 1. 0, $1.0/\sqrt{\tilde{G}_L}$ -0. 01.

For each experiment of inter array, a set of $\tilde{Z}_i$ can be determined. Then L_i can be determined with respect to STEP 1.

2) Select $L_{27}(3^{13})$ as error array (also called external array) and the above $\tilde{Z}_1$, L_i, i=1, 2, 3 as the factors for external array experiment. With the assuming +-10% tolerance, select the three levels of each factor as 0. 9N, N, 1. 1N, N denotes the nominal value of the factor. For each experiment of error array, calculate the following evaluation function E:

$$E=(|\Gamma_{in}|/|\Gamma_{ino}|)^2 \qquad (3)$$

where $|\Gamma_{ino}|$ is the reflection coeffient specification of the matching network. In this work, $20\log_{10}(|\Gamma_{ino}|)$=-25 dB.

3) Calculate the average of E's, namely Ea, and return to optimizing array with Ea. For optimizing array, analyze all Ea's according to the method of [4] and determine the best combination of $\tilde{Z}_i$ according to the rule:

The smaller Ea is, the higher the yield is.

To determine the high yield topologies of matching networks, the Smith Chart is divided into four regions as shown in Fig. 2, 100 $\tilde{Z}_L$'s which are uniformly distributed on it are selected and each matching network of Fig. 1 is used to match $\tilde{Z}_L$. Then Monte Carlo simulation is exploited to estimate the corresponding yield and verify the above rule. Some results are listed in Table 1.

From Table. 1, two conclusions can be drawn:

1) For the given $\tilde{Z}_L$, the topology of the matching network strongly effects its yield;

2) Ea can be used as a yield measure for yield improvement and time-consuming Monte Carlo simulation can be avoided.

Summary all the results, the high yield topologies of the matching networks as shown in Fig.1 for the four different load impedance regions are provided in Fig.2.

With respect to the characters of the open-terminated and short-terminated transmission line, the mixed lumped-distributed matching network of Fig. 3 can be easily derived from the distributed one of Fig. 1. The design method is similar. For each topolgy, the above 100 $\tilde{Z}_L$'s are used for yield study. Summary all the results, the high yield topologies for the different load impedance regions are also provided in Fig. 2.

In short, for a given $\tilde{Z}_L$, the design approach for the high yield matching network is

1. Select the high yield topology according to Fig. 2

2. Use orthogonal array $L_9(3^4)$ as optimizing array, select $\tilde{Z}_1$ as factors, and determine the three levels of each factor appropriately.

3. For a specific set of $\tilde{Z}_i$, determine L_1 with respect to STEP 1.

4. Use orthogonal array $L_{27}(3^{13})$ as error array, select the above $\tilde{Z}_i$, L_1, i=1, 2, 3 as factors and determine the three levels of each factor according to the tolerances. For each experiment of error array, calculate the evaluation function E and return to optimizing array with the average of E's, i. e., Ea.

5. In optimizing array, analyze all the Ea's according to the method of [4] and select the best level combination of factors.

6. If do not satisfy, redefine the levels of each factor of optimizing array, repeat step 2, 3, 4, 5.

3. HIGH YIELD FET AMPLIFIER DESIGN

It is well known that the core of the FET amplifier design is the input and output matching networks design. For the given FET, the high yield matching topologies must be used for high yield amplifier design.

In this paper, a single-stage FET amplifier is designed. First, the FET S parameters of [5] are used as means and +-5% as tolerances to establish an S parameter database.In the database, all S11's and S22's are located at region 1 and 3 of Fig.2 respectively. So the topologies of Fig.1(b) and (a) are used for the input and output matching networks design. At the center frequency 12GHz, the input and output matching networks are designed with respect to the approach of Section 2.Then, the results are taken as the initial values for the whole amplifier design. Finally, the amplifier is designed as follow:

1. Select $L_{27}(3^{13})$ for OAE and take the characteristic impedances of the input and output matching networks as the factors of OAE.

2. Take the 70%, 100%, 130% of the initial value as the three levels of each factor respectively.

3. Take the yield of the amplifier as the evaluation fuction for OAE, i. e.

$$\text{Yield} = (1/m)\sum_{i=1}^{m}\delta(X_1) \qquad (4)$$

where

$$\delta(X_1) = \begin{cases} 1 & \text{if } (1/n)\sum_{j=1}^{n}\delta_j^{(1)} = 1 \\ 0 & \text{if } (1/n)\sum_{j=1}^{n}\delta_j^{(1)} < 1 \end{cases}$$

$$\delta_j^{(i)} = \begin{cases} 1 & \text{if } \rho_{in}^{(i)}(f_j) <= 2.5 \text{ and } G^{(i)}(f_j) >= 2.5\text{dB} \\ 0 & \text{otherwise} \end{cases}$$

where m (m=1000) is the total number of the circuit simulations; i is the orders of m; n (n=6) is the total number of the frequencies to be analyzed in the band; J is the order of n; $\rho_{in}^{(i)}(f_j)$ and $G^{(i)}(f_j)$ are the input VSWR and gain of the ith circuit simulation at the Jth frequency. X_1 is the vector of the amplifier paremeters:

$$X_i = (\tilde{Z}_{1i}, L_{1i}, S11, S12, S21, S22, \tilde{Z}_{2i}, L_{2i})T \qquad (5)$$

$$i=1,\ 2,\ 3$$

When the yield is estimated, the parameters of the matching network are all assumed as the uniform distributed, indepedent random varibles with +-5% tolerance and S parameters are selected randomly from the established database.

4. Select the best level combination of factors, i. e. $\tilde{Z}_{1i}$ and $\tilde{Z}_{2i}$, i=1, 2, 3, for the matching network design and obtain L_{1i}, L_{2i}. The final amplifier, namely AMP1, is shown in Fig. 4.

In order to compare with the amplifier of [5], namely AMP2, the gain, VSWR and the yield of AMP1 and AMP2 are listed in table 2. From table 2, both of them have the similar gain and VSWR, but AMP1 has a much higher yield than AMP2.

4. CONCLUSION

The main idea of OAE is using two orthogonal arrays as optimizing array and error array. For each set of factors in optimizing array, use error array to perturb it orderly and obtain the average of the evaluation function Ea.According to optimizing array and all Ea's, determine the best factor level combination.With this new effective approach , high yield matching network can be designed and the high yield topologies for the load impedances located at the different regions on the Smith Chart can be determined conveniently.Also with OAE , a high yield single-stage FET amplifier is designed.Its yield (65.6%) is much higher than that of the amplifier of [5] (42.4%).

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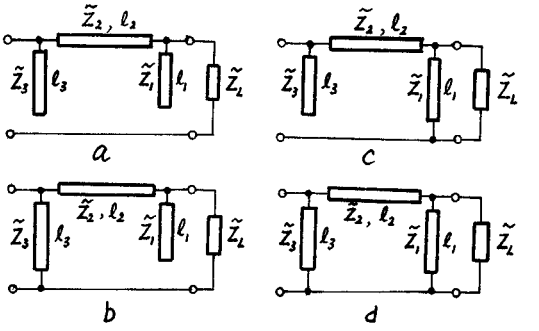

Fig. 1 Distributed π Matching Network

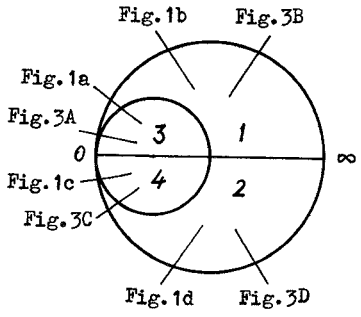

Fig. 2 Load Impedance Regions and High Yield Topologies

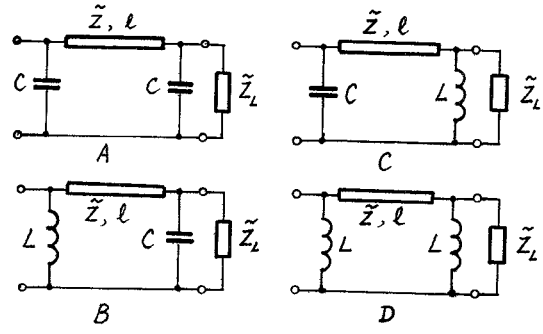

Fig. 3 Lumped-Distributed π Matching Network

Table 1. Some Results of Yield Study by OAE and Monte Carlo Simulation

Load Impedance	Region	Struc.a		Struc.b		Struc.c		Struc.d	
		Ea	Y(%)	Ea	Y(%)	Ea	Y(%)	Ea	Y(%)
0.71+j0.71	1	4.59	29.6	3.03	44.2	15.75	9.4	14.21	14.21
1.3+j0.65	1	3.94	31.4	2.56	50.6	6.99	19.2	5.62	24.8
0.71-j0.71	2	17.07	9.0	16.66	13.4	4.73	29.6	3.29	44.0
1.3-j0.65	2	8.56	17.8	7.28	21.0	4.36	30.2	3.14	38.4
0.62+j0.31	3	0.93	88.0	2.37	54.2	3.93	37.8	5.31	30.1
0.62-j0.31	4	4.55	45.4	5.96	28.2	1.06	82.0	2.59	50.4
0.5+j0.25	3	1.58	69.6	3.06	40.0	4.64	34.6	6.5	21.8
0.5-j0.25	4	5.09	37.8	6.89	21.8	1.70	68.6	3.38	41.0

Table 2. Comparison between AMP1 and AMP2

FREQ (CHZ)	VSWR		GAIN(dB)		YIELD(%)	
	AMP1	AMP2	AMP1	AMP2	AMP1	AMP2
11.7	1.93	1.52	3.36	3.71	65.6	42.4
11.8	1.55	1.35	4.25	4.14		
11.9	1.25	1.32	4.48	4.23		
12.0	1.22	1.54	4.63	4.27		
12.1	1.55	1.95	4.60	4.13		
12.2	2.04	2.52	4.23	3.68		

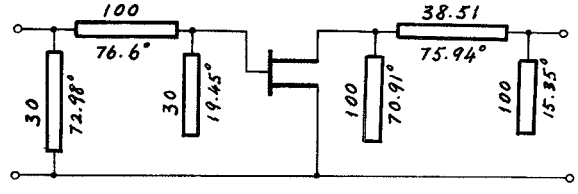

Fig. 4 High Yield FET Amplifier